

Fabrication of Pure-semiconducting Single-walled Carbon Nanotube Arrays and Nanotube Transistors

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Single-walled carbon nanotube (SWNT) is a promising material of electronic devices for next generation. However, as-grown SWNTs are usually a mixture of semiconducting and metallic ones. Therefore, purification or separation processes are always needed to fabricate SWNT transistors with high performance. Here, we performed the removal of metallic SWNTs (m-SWNTs) from horizontally-aligned SWNTs (HA-SWNTs) [1-3] and fabricate SWNT transistors.

First, horizontally-aligned SWNTs were synthesized on a crystal quartz substrate and they were transferred onto a silicon substrate, as shown in Fig. 1(A). Second, the SWNTs were connected with a pair of electrodes and they were heated by Joule-heating in the air-ambient. Heated SWNTs were partially oxidized and broken down with forming nano-gaps. Third, voltage was applied between the electrodes in the saturated water vapor pressure after coating of an organic film, and then the broken SWNTs on the anode side were shrunk. Because the nano-gap formation occurs in only m-SWNTs, it is expected that a large portion of m-SWNTs were removed from the arrays. Next, SWNT transistors were fabricated in order to confirm the electric conductivity of the removed SWNTs. In this case, by making the nano-gaps near the cathode, almost the all parts of broken SWNTs were removed, as shown in Fig. 1(B). The SWNT transistors exhibit high on/off ratio which indicates that purely semiconducting SWNT arrays are obtained using the m-SWNT removal technique. In the presentation, we will show the details of the removal techniques and discuss their mechanism.

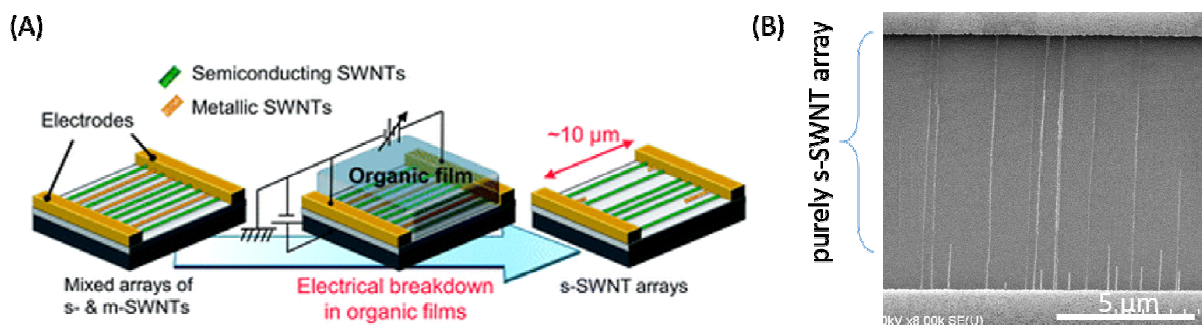


Fig. 1: (A) Removal process of m-SWNTs from horizontally-aligned SWNTs . (B) SEM image of purely s-SWNT array.

[1] K. Otsuka, T. Inoue, S. Chiashi, S. Maruyama, *Nanoscale*, **6**, 8831 (2014).

[2] K. Otsuka, T. Inoue, Y. Shimomura, S. Chiashi and S. Maruyama, *Nanoscale*, **8**, 16363 (2016).

[3] K. Otsuka, T. Inoue, Y. Shimomura, S. Chiashi and S. Maruyama, *Nano Res.* (to be published).